20th IEEE International Conference on
Application-specific Systems, Architectures and Processors
Boston MA, USA, July 7-9, 2009

Sponsored by

ASAP 2009: Advance Program

Sessions: Room Carver 1 and 2
Lunches & Receptions: Room Carver 3

Tuesday July 7, 2009

7:45am Breakfast and Registration

8:15am - 8:30am Welcome

8:30am - 9:30am Keynote Speech

Grand Challenges in Computational Systems Biology
Dr. Jeffrey Skolnick
Georgia Institute of Technology

9:30am - 10:45am Session 1: Arithmetic

Chair: *Milos Ercegovac*, UCLA

Division Unit for Binary Integer Decimals
Tomas Lang[1] and Alberto Nannarelli[2]
[1]UC Irvine, [2]Technical Univ. of Denmark

A Combined Decimal and Binary Floating-point Multiplier
Charles Tsen[1], Sonia Gonzalez-Navarro[2], Michael Schulte[1], Brian Hickmann[3], Katherine Compton[1]
[1]University of Wisconsin - Madison, [2]Universidad de Málaga, [3]Intel Corporation

Parallel Prefix Ling Structures for Modulo 2^n - 1 Addition
Jun Chen and James Stine
Oklahoma State University

10:45am - 11:15am Break / View Posters

Integral Parallel Architecture & Berkeley's Motifs
Mihaela Malita[1] and Gheorghe Stefan[2]
[1]Saint Anselm College, NH, [2]BrightScale, CA

Application Specific Transistor Sizing for Low Power Full Adders
Amirali Baniasadi
University of Victoria

Reconfigurable SWP Operator for Multimedia Processing
Shafqat Khan, Emmanuel Casseau, Daniel Menard
IRISA INRIA

Filtering Global History: Power and Performance Efficient Branch Predictor
Raid Ayoub, Alex Orailoglu
University of California, San Diego

Efficient Implementation of Carry-Save Adders in FPGA
Javier Hormigo[1], Manuel A. Ortiz[2], Francisco Quiles[2], Francisco J. Jaime[1], Julio Villalba[1], Emilio L. Zapata[1]
[1]University of Malaga, [2]University of Cordoba

Acceleration of Multiresolution Imaging Algorithms: A Comparative Study
Richard Membarth, Philipp Kutzer, Hritam Dutta, Frank Hannig, Juergen Teich
University of Erlangen-Nuremberg

11:15am - 12:05pm Session 2: FPGA Applications I

Chair: *Xinming Huang*, Worcester Polytechnic Institute

A FPGA-based Parallel Architecture for Scalable High-Speed Packet Classification
Weirong Jiang and Viktor Prasanna
University of Southern California

Implementing a Highly Parameterized Digital PIV System On Reconfigurable Hardware
Abderrahmane Bennis, Miriam Leeser, Gilead Tadmor
Northeastern University

12:05pm - 2:00pm Lunch / View Posters

2:00pm - 3:15pm Session 3: Media and Image Processing

Chair: *Mark Franklin*, Washington University in St. Louis

Improving VLIW Processor Performance using Three-Dimensional (3D) DRAM Stacking
Yangyang Pan and Tong Zhang
Rensselaer Polytechnic Institute

Specialization of the Cell SPE for Media Applications
Cor Meenderinck and Ben Juurlink
Delft University of Technology

A Massively Parallel Coprocessor for Convolutional Neural Networks
Murugan Sankaradas, Venkata Jakkula, Srihari Cadambi, Srimat Chakradhar, Igor Durdanovic, Eric Cosatto, Hans Peter Graf
NEC Laboratories America, Inc.

3:15pm - 3:45pm Break / View Posters

3:45pm - 5:00pm Session 4: FPGA Applications II

Chair: *Martin Herbordt*, Boston University

An FPGA-based Parallel Hardware Architecture for Real-time Face Detection using a Face Certainty Map
Seunghun Jin[1], Dongkyun Kim[1], Thuy Toung Nguyen[1], Bongjin Jun[2], Daijin Kim[2], Jae Wook Jeon[1]
[1]Sungkyunkwan Univ., [2]Postech

Accelerating a Virtual Ecology Model with FPGAs
Julien Lamoureux, Tony Field, Wayne Luk
Imperial College

Parallelized Architecture of Multiple Classifiers for Face Detection
Junguk Cho[1], Bridget Benson[1], Shahnam Mirzaei[2], Ryan Kastner[1]
[1]University of California, San Diego, [2]University of California, Santa Barbara

5:30pm-10pm Harbor Cruise

***** Bus Boarding at 5:30pm *****

Wednesday July 8, 2009

8:00am Registration & Breakfast

8:30am - 9:30am Keynote Speech

Got Game? Experiences with a Cluster of Over 330 PS3s
Dr. Richard Linderman
Air Force Research Laboratory

9:30am - 10:45am Session 5: Arithmetic and Cryptography

Chair: *James Stine*, Oklahoma State University

Design and Implementation of a Radix-4 Complex Division Unit with Prescaling
Pouya Dormiani[1], Milos Ercegovac[1], Jean-Michel Muller[2]
[1]University of California at Los Angeles, [2]Ecole Normale Superieure de Lyon

A Low Power High Performance Radix-4 Approximate Squaring Circuit
Satyendra Datla[1], Mitchel Thornton[2], David Matula[2]
[1]TI, Dallas TX, [2]SMU, Dallas, TX

A Novel Processor Architecture for McEliece Cryptosystem and FPGA Platforms
Abdulhadi Shoufan[1], Thorsten Wink[1], Gregor Molter[1], Sorin Huss[1], Falko Strenzke[2]
[1]TU Darmstadt, [2]Flexsecure

10:45am - 11:15am Break / View Posters

An Efficient Hardware Architecture for Spectral Hash Algorithm
Ray C.C. Cheung[1], Cetin Kaya Koc[2], John D. Villasenor[1]
[1]UCLA, [2]UCSB

P3FSM: Portable Predictive Pattern Matching Finite State Machine
Lucas Vespa, Mini Mathew, Ning Weng
Southern Illinois University

Run-Time Detection of Malwares via Dynamic Control-Flow Inspection
Yong-Joon Park[1], Zhao Zhang[1], Songqing Chen[2]
[1]Department of Electrical and Computer Engineering, Iowa State University, [2]Department of Computer Science, George Mason University

A Sixteen-context Optically Reconfigurable Gate Array
Mao Nakajima and Minoru Watanabe
Shizuoka University

Mapping Parallel FFT Algorithm onto SmartCell Coarse-Grained Reconfigurable Architecture
Cao Liang and Xinming Huang
Worcester Polytechnic Institute

An Area-Efficient LDPC Decoder Architecture and Implementation for CMMB Systems
Kai Zhang[1], Xinming Huang[1], Zhongfeng Wang[2]
[1]Worcester Polytechnic Institute, [2]Broadcom Corporation

11:15am - 12:05pm Session 6: Application-Specific Integrated Circuits

Chair: *Frank Hannig*, University of Erlangen-Nuremberg

An Input Triggered Polymorphic ASIC for H.264 Decoding
Adarsha Rao[1], Mythri Alle[1], Sainath V[1], Reyaz Shaik[1], Rajashekhar Chowhan[1], Sankaraiah S[1], Sravanthi Mantha[1], Nandy S. K.[1], Ranjani Narayan[2]
[1]Indian Institute of Science, [2]Morphing Machines Pvt. Ltd.

Power-scalable Reconfigurable Switch-Based FFT Processor
Bassam Mohd[1] and Earl Swartzlander, Jr.[2]
[1]Qualcomm, Inc, [2]University of Texas-Austin

12:05pm - 1:30pm Lunch / View Posters

1:30pm - 2:00pm Invited Talk

FPGA-based RTL Emulation for Embedded Software Development
Rich Claggett
EVE-USA

2:00pm - 3:15pm Session 7: Computational Biology

Chair: *Jeremy Buhler*, Washington University in St. Louis

MSA-CUDA: Multiple Sequence Alignment on Graphics Processing Units with CUDA
Yongchao Liu, Bertil Schmidt, Douglas Maskell
School of Computer Engineering, Nanyang Technolgical University, Singapore 639798

Parallel Discrete Event Simulation of Molecular Dynamics Through Event-Based Decomposition
Martin Herbordt, Ashfaq Khan, Tony Dean
Boston University

NeMo: A Platform for Neural Modelling of Spiking Neurons Using GPUs
Andreas Fidjeland, Etienne Roesch, Murray Shanahan, Wayne Luk
Imperial College London

3:15pm - 3:45pm Break / View Posters

3:45pm - 5:15pm Panel Session

Multi-Core/Threaded Processors vs Diverse Component Integrated Systems
Organizer: *Mark Franklin,* Washington Univ. in St. Louis
Panelists: *Wayne Luk,* Imperial College, London
Brian Ogilvie, Mathworks
Jeremy Buhler, Washington Univ. in St. Louis
Jay Wilkinson, Intel
Michael Champigny, Mercury Computer Systems

6:00pm - 8:00pm Demo Night

Thursday July 9, 2009

8:00am Registration & Breakfast

8:30am - 9:45am Session 8: Tools and Design Aids

Chair: *Xinming Huang*, Worcester Polytechnic Institute

Constraint-Driven Instructions Selection and Application Scheduling in the DURASE system
Kevin Martin[1], Christophe Wolinski[1], Krzysztof Kuchcinski[2], Antoine Floch[1], Francois Charot[1]
[1]University of Rennes I, Irisa, Inria, France, [2]Dept. of Computer Science, Lund University, Sweden

A System Framework for the Design of Embedded Software Targeting Heterogeneous Multi-Core SoCs
Xavier Guérin and Frédéric Pétrot
TIMA Laboratory

Impact of Loop Tiling on the Controller Logic of Hardware Acceleration Engines
Hritam Dutta, Jiali Zhai, Frank Hannig, Juergen Teich
University of Erlangen-Nuremberg

9:45am - 10:15am Break

10:15am - 11:30am Session 9: Application-Specific Instruction Processors

Chair: *Miriam Leeser*, Northeastern University

Evaluating Various Branch-Prediction Schemes for Biomedical-implant Processors
Christos Strydis and Georgi Gaydadjiev
TU Delft

Low-Power ASIP Architecture Exploration and Optimization for Reed-Solomon Processing
Andreas Genser[1], Christian Bachmann[1], Christian Steger[1], Jos Hulzink[2], Mladen Berekovic[3]
[1]Institute for Technical Informatics, Graz University of Technology, Austria, [2]IMEC NL,

Holst Centre Eindhoven, The Netherlands, [3]Technical University Braunschweig, Germany

Scalar Processing Overhead on SIMD-Only Architectures
Arnaldo Azevedo and Ben Juurlink
TU Delft

11:30am - 11:45pm Wrap-Up